WHAT IS CLAIMED IS:

1. A packet switch comprising:

an input buffer memory unit having a logic queue corresponding to an output line;

a control module for a first pointer indicating a scheduling start input line;

a control module for a second pointer indicating a scheduling start output line of scheduling target outlines;

a request management control module for retaining transmission request data about a desired output line;

a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer, and selecting an output line that is not ensured by other input lines;

a packet buffer memory unit for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets;

a common switch unit for switching the fixed-length packets outputted from said packet buffer memory unit; and

an address management unit for segmenting an address of said packet buffer memory unit into fixed-length blocks for a plurality of packets, and managing the address on a block basis.

2. A packet switch comprising:

an input buffer memory unit having a logic queue corresponding to an output line;

a control module for a first pointer indicating a

scheduling start input line;

a control module for a second pointer indicating a scheduling start output line of scheduling target outlines;

a request management control module for retaining transmission request data about a desired output line;

a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer selecting an output line that is not ensured by other input lines;

a packet buffer memory unit for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets;

a common switch unit for switching the fixed-length packets outputted from said packet buffer memory unit; and

an address management unit for temporarily writing the packets to a multicast-oriented memory for multicasting to a plurality of output lines, reading the packets corresponding to the number of multicasts, with a scheme to distribute the packets to a desired FIFO memory, retaining the number of multicasts and addresses thereof according to the addresses after being distributed in order to logically actualize the distribution of not the packets but by use of only the addresses, and thus making an address management of said packet buffer memory unit.

3. A packet switch according to claim 1, wherein said address management unit manages the addresses by flags indicating

which sequence number in the block and which address related to this indicated sequence number the multicast is completed with.

claim 1

a 4. A packet switch ~~according to claim 1 or 2~~, wherein said packet buffer memory unit has a large-capacity memory that is high-speed accessible only when in a burst access and is disposed at a front stage, and a high-speed random accessible memory disposed at a rear stage,

only said rear-stage memory is normally used,

when said rear-stage memory is full of packet data, the packet data are temporarily stored in said front-stage memory, and

the packet data are transferred back to said rear-stage memory when a free area comes out.

claim 1

a 5. A packet switch ~~according to claim 1 or 2~~, wherein said packet buffer memory unit has a queue memory using a small-capacity high-speed random accessible memory disposed at a front stage, and a large-capacity low-speed access memory disposed in parallel at a rear stage,

a writing operation to said rear-stage memory is effected in parallel from said front-stage memory, and

a reading operation from said rear-stage memory is effected by selecting only a queue memory with no conflict.

claim 3

a 6. A packet switch ~~according to claim 1 or 2~~, wherein said

packet buffer memory unit has a queue memory using a small-capacity high-speed random accessible memory disposed at a front stage, and a queue memory using a large-capacity memory that is high-speed accessible only when in a burst access and disposed at a rear stage,

a writing operation to said rear-stage memory is effected batchwise just when a plurality of packets are accumulated in said front-stage memory, and

the plurality of packets are read batchwise from said rear-stage memory.

7. A packet switch ~~according to claim 1 or 2~~ claim 1, wherein said packet buffer memory executes time-division-multiplexing of the fixed-length packets of the plurality of input lines onto one signal input line in an established manner, and includes memories disposed in parallel corresponding to every input line before being multiplexed, and

the writing and reading to and from said respective memories are executed in parallel.

8. A packet switch ~~according to claim 1 or 2~~ claim 1, wherein said common switch unit is based on a bit-slice architecture and has slice switches of which at least one slice switch is used as a redundant switch, and

switching to said redundant slice switch can be thereby done every time said slice switch receives maintenance and comes to a fault.

9. A packet switch ~~according to claim 1 or 2,~~ Claim 1 wherein said packet buffer memory unit is set dual on the input side and the output side of said common switch unit,

packet data are distributed to said packet buffer memory unit disposed on the output side along a route preset in said common switch unit, and

the switching can be thereby done when in maintenance and in fault.

10. A packet switch ~~according to claim 1 or 2,~~ Claim 1 wherein schedulers each including said control modules of the first and second pointers, said request management control module and said scheduling processing module, are disposed in dispersion,

a switch unit for selecting scheduling data between adjacent input buffer units among said input buffer units including said input buffer memory units, is further provided, and

the switching can be thereby done when in maintenance and in fault.

11. A packet switch comprising:

an input buffer memory unit having a logic queue corresponding to an output line;

a control module for a first pointer indicating a scheduling start input line;

a control module for a second pointer indicating a

scheduling start output line of scheduling target outlines;

a request management control module for retaining transmission request data about a desired output line;

a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer, and selecting an output line that is not ensured by other input lines;

a packet buffer memory unit for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets;

a common switch unit for switching the fixed-length packets outputted from said packet buffer memory unit; and

an address management unit for performing an address management of said packet buffer memory unit,

wherein said packet buffer memory unit has a large-capacity memory that is high-speed accessible only when in a burst access and is disposed at a front stage, and a high-speed random accessible memory disposed at a rear stage,

only said rear-stage memory is normally used,

when said rear-stage memory is full of packet data, the packet data are temporarily stored in said front-stage memory, and

the packet data are transferred back to said rear-stage memory when a free area comes out.

12. A packet switch comprising:

an input buffer memory unit having a logic queue

corresponding to an output line;

a control module for a first pointer indicating a scheduling start input line;

a control module for a second pointer indicating a scheduling start output line of scheduling target outlines;

a request management control module for retaining transmission request data about a desired output line;

a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer, and selecting an output line that is not ensured by other input lines;

a packet buffer memory unit for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets;

a common switch unit for switching the fixed-length packets outputted from said packet buffer memory unit; and

an address management unit for performing an address management of said packet buffer memory unit,

wherein said packet buffer memory unit has a queue memory using a small-capacity high-speed random accessible memory disposed at a front stage, and a large-capacity low-speed access memory disposed in parallel at a rear stage,

a writing operation to said rear-stage memory is effected in parallel from said front-stage memory, and

a reading operation from said rear-stage memory is effected by selecting only a queue memory with no conflict.

13. A packet switch comprising:

an input buffer memory unit having a logic queue corresponding to an output line;

a control module for a first pointer indicating a scheduling start input line;

a control module for a second pointer indicating a scheduling start output line of scheduling target outlines;

a request management control module for retaining transmission request data about a desired output line;

a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer, and selecting an output line that is not ensured by other input lines;

a packet buffer memory unit for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets;

a common switch unit for switching the fixed-length packets outputted from said packet buffer memory unit; and

an address management unit for performing an address management of said packet buffer memory unit,

wherein said packet buffer memory unit has a queue memory using a small-capacity high-speed random accessible memory disposed at a front stage, and a queue memory using a large-capacity memory that is high-speed accessible only when in a burst access and disposed at a rear stage,

a writing operation to said rear-stage memory is effected batchwise just when a plurality of packets are accumulated in

said front-stage memory, and

the plurality of packets are read batchwise from said rear-stage memory.

14. A packet switch comprising:

an input buffer memory unit having a logic queue corresponding to an output line;

a control module for a first pointer indicating a scheduling start input line;

a control module for a second pointer indicating a scheduling start output line of scheduling target outlines;

a request management control module for retaining transmission request data about a desired output line;

a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer, and selecting an output line that is not ensured by other input lines;

a packet buffer memory unit for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets;

a common switch unit for switching the fixed-length packets outputted from said packet buffer memory unit; and

an address management unit for performing an address management of said packet buffer memory unit,

wherein said packet buffer memory executes time-division-multiplexing of the fixed-length packets of the plurality of input lines onto one signal input line in an

established manner, and includes memories disposed in parallel corresponding to every input line before being multiplexed, and

the writing and reading to and from said respective memories are executed in parallel.

claim 11

15. A packet switch ~~according to claim 11, 12, 13 or 14,~~ wherein said common switch unit is based on a bit-slice architecture and has slice switches of which at least one slice switch is used as a redundant switch, and

switching to said redundant slice switch can be thereby done every time said slice switch receives maintenance and comes to a fault.

claim 11

16. A packet switch ~~according to claim 11, 12, 13, 14 or~~ 15, wherein said packet buffer memory unit is set dual on the input side and the output side of said common switch unit,

packet data are distributed to said packet buffer memory unit disposed on the output side along a route preset in said common switch unit, and

the switching can be thereby done when in maintenance and in fault.

claim 11

17. A packet switch ~~according to claim 11, 12, 13, 14, 15~~ or 16, wherein schedulers each including said control modules of the first and second pointers, said request management control module and said scheduling processing module, are disposed in dispersion,

a switch unit for selecting scheduling data between adjacent input buffer units among said input buffer units including said input buffer memory units, is further provided and

the switching can be thereby done when in maintenance and in fault.

18. A packet switch comprising:

a scheduling processing module for executing a scheduling process at a certain fixed speed;

a first timer processing module for measuring a packet slot time obtained from a scheduling speed for an input line speed; and

a second timer processing module for measuring a packet slot time obtained from a scheduling speed for an output line speed,

wherein when the scheduling process for a certain input line is executed, said first timer processing module starts the measurement,

the scheduling process for that input line is stopped during a period for which said first timer processing module thereafter measures a predetermined time, and

the scheduling corresponding to the input line speed is thus actualized.

19. A packet switch according to claim 18, wherein when an establishment for a certain output line is made, said second

timer processing module starts the measurement,

the establishment for the same output line is stopped during a period for which said second timer processing module thereafter measures a predetermined time, and

a traffic flow to the same output line is restrained to an output line speed or lower.

20. A packet switch according to claim 18, wherein the start of the measurement of each of said first and second timer processing modules is triggered neither by scheduling nor by the establishment but by a fixed time interval.

21. A packet switch according to claim 18, wherein when the scheduling process is executed in a way of pipeline processing, the scheduling for a relevant input line at pipeline processing N-stages anterior and posterior on the basis of a ratio of a scheduling speed to an input line speed, is stopped, and

the scheduling corresponding to the input line speed is thereby actualized.

22. A packet switch according to claim 18, wherein said second timer processing module, when executing the scheduling process in a way of pipeline processing, executes the control independently for every pipeline process on the basis of a pipeline number and an output line number, and

the scheduling corresponding to the respective output line speed on the average is actualized by keeping a predetermined

interval in each pipeline process.